UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,318	03/09/2004	Jeng-Jye Shau	SHAU-0303	2124

50887 7590 05/22/2006

JENG-JYE SHAU
991 AMARILLO AVE.
PALO ALTO, CA 94303

EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,318	SHAU, JENG-JYE	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1 and 4** are rejected under 35 U.S.C. 102(e) as being anticipated by Kurchuk (US 2002/0101641).

3. Regarding claim **1**, Kurchuk discloses in Fig 4 an electrical circuit comprising: a plurality of voltage controlled capacitors (404, 406, ¶34) with different capacitance values (¶36) in different ranges of bias voltages (¶36); a plurality of input signals (through 428, 430) connected to said capacitors; an output signal (into 422) connected to the capacitors; and a sensing circuit (422) connected to the output signal, and the output of said sensing circuit is determined by the coupling voltages between said input signals and said output signal through said capacitors (¶45).

4. Regarding claim **4**, Kurchuk discloses in Fig 4A wherein the circuit of claim 1 is an optical sensor (item 418, ¶44).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **5-6 and 8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurchuk and Ogawa (US 2005/0127411).

7. Regarding claim **6**, Kurchuk discloses the circuit of claim 1, but does not specify that the circuit uses MOS devices as voltage-controlled capacitors, said MOS devices comprising: a semiconductor substrate; a thin film insulator layer deposited on said semiconductor substrate; and a conductor layer deposited on said thin film insulator layer.

Ogawa teaches a MOS type variable capacitance device that can be manufactured with ease by a general manufacturing process for semiconductor circuit devices (¶3). As taught in Fig 2a, the MOS devices comprise a substrate (2), a thin film insulator layer (4) on the substrate, and a conductor layer (6) deposited on the insulator layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ogawa on the structure of Kurchuk in order to replace the analog varactors and use the same ordinary manufacturing steps for both semiconductor integrated circuits and variable capacitance devices (¶3 and 47).

8. Regarding claim **8**, Kurchuk and Ogawa disclose wherein the circuit in claim 6 is an electrical optical sensor (Kurchuk ¶44).

9. Regarding claims **5 and 9**, Ogawa discloses wherein the circuit in claims 1 and 6 shares the same area with other active devices to form a 3 dimensional device (Ogawa Fig 5).

10. Regarding claim **10**, Ogawa discloses in Fig 1 wherein the circuit in claim 6 has a p-type semiconductor substrate (2).

11. Regarding claim **11**, Ogawa discloses in Fig 15 wherein the circuit in claim 6 has an n-type semiconductor substrate (201).

12. Claims **12 and 15-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurchuk and Hyde (US 2004/0206999).

13. Regarding claim **12**, Kurchuk discloses the circuit of claim 1, but does not specify wherein the circuit uses floating gate devices as voltage controlled capacitors, said floating gate devices comprising: a semiconductor substrate; a thin film insulator layer on said substrate; a floating gate deposited on said thin film insulator layer; a second thin film insulator on said floating gate; and a conductor layer on said second thin film, insulator.

Hyde teaches the desirability of implementing a floating gate variable capacitance device (such as a varactor) in standard CMOS technique, in order to avoid modification of the standard CMOS processing and keep fabrication expenses low (¶2 and 3). The floating gate variable capacitor as taught by Hyde in Fig 7 includes each of the elements claimed, including a floating gate (62) and a second conductor layer (64). It would have been obvious to one of ordinary skill in the art at the time of the invention

to use the teachings of Hyde and replace the varactors on Kurchuk's device with floating gate capacitors, in order to avoid modification of standard CMOS processes.

14. Regarding claim **15**, Kurchuk discloses wherein the circuit in claim 12 shares the same area with other active devices to form a 3 dimensional device (Fig 7).

15. Regarding claim **16**, Kurchuk discloses in Fig 7 wherein the circuit of claim 12 has a p-type semiconductor substrate.

16. Regarding claim **17,** Kurchuk discloses in Fig 7 wherein the circuit of claim 12 has a p-type substrate. It is obvious to one of ordinary skill in the art that MOS devices can be populated on either n-type substrate or on p-type substrates.

17. Regarding claim**18**, Kurchuk discloses in Fig 7 wherein the device of claim 12 has source and drain regions (two p+ regions) to form a floating gate transistor (along with floating gate 62 and control gate 64).

18. Regarding claim **19**, Hyde discloses in the abstract that floating gate MOS capacitors may be connected in series (NAND configuration) in order to reduce the nonlinearity of the capacitances.

19. Claim **20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurchuk and Hyde as applied to claim18 above, and further in view of Ogawa.

20. Regarding claim **20,** Kurchuk and Hyde disclose the floating gate transistor of claim 18, but do not specify wherein the transistors are connected in parallel NOR configuration.

Ogawa teaches in Figs 3 and 4 that MOS type variable capacitors can be connected in or parallel, which matches the NOR configuration as claimed, in order to improve the linearity of the variable capacitance device (¶46). It would have been obvious to one of ordinary skill in the art to improve the linearity of the MOS variable capacitance device by connecting the capacitors in parallel configuration (NOR).

21. Claims **2-3 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurchuk and Ogawa as applied to claims 1 and 6 above, and further in view of Steele (US 5,309,046).

Kurchuk and Ogawa disclose the circuits of claims 1 and 6, but fail to specify wherein the circuit is a memory device or a programmable logic array. However, Steele teaches that PLAs (a memory device) may be made of floating gate MOS devices, such as those taught by Ogawa, because of more flexibility in programming (col 1 ln 46-50). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Steele on the device of Kurchuk and Ogawa in order to ensure good programming flexibility.

22. Claims **13 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurchuk and Hyde as applied to claim 12 above, and further in view of Broze (US 5,633,518).

Regarding claims **13 and 14,** Kurchuk and Hyde disclose the circuit of claim 12, but fail to specify wherein the circuit is a memory device or a field programmable logic

circuit. However, Broze teaches that floating gate MOS transistors may be used as FPGAs (a memory device) because of their nonvolatile re-programmability (col 1 ln 34-36). It would have been obvious to one of ordinary skill in the art to use the teachings of Broze on the structure of Kurchuk and Hyde in order to utilize them for floating gate memory/ FPGAs with nonvolatile re-programmability characteristics.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER